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EXAMINER	
GOLE, AMOL V	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,403	BURCH, CARL D.	
	Examin r	Art Unit	
	Amol V. Gole	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/30/01,9/19/01*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Receipt is acknowledged of the following papers:

1) IDS (9/19/01)

These papers have been placed of record in the file.

2. Claims 1-20 have been examined.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following limitations must be shown or the feature(s) canceled from the claim 19 and 20:

a) an indicating means; and

b) an instruction queue.

No new matter should be entered.

4. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 8 and 9 are objected to because of the following informalities:

a) On line 2 of claims 8, 9, 17 and 18 the word "of" should be inserted between the words "processing the". Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims **1-9, 19, and 20** are rejected under 35 U.S.C. 102(b) as being anticipated by Smith and Pleszkun ("Implementing Precise Interrupts In Pipelined Processors," IEEE Trans. On Comp., Vol. 37, No. 5, May 1988, pp. 562-573).

8. In regard to claim 1:

9. Smith et al. disclose a method for retiring instructions processed through various processing stages (pipeline stages, fig. 1), comprising the steps of:

a) processing an instruction capable of early retirement (pipeline processes instructions capable of retiring out-of-order due to parallel execution of instructions [col. 5, para. 4, lines 1-7]) in functional units with varying execution times [col. 5-6, example 1 indicates varying execution times of the functional

units]) until the instruction meets the criteria for early retirement (when an instruction reaches stage 1 of the result shift register [col. 7, para. 4, last 4 lines]).

b) indicating that the instruction has met the early-retirement criteria (functional unit result is placed in the correct result register [col. 7, para. 4, last 4 lines]);

c) processing the instruction to a desirable stage (result shift register, [col. 7, para. 4]) at which, based on the indication the instruction has met the early-retirement criteria (result is placed in the correct result register, [col. 7, para. 4, last 4 lines]), the instruction is terminated out of order of a program running the instruction (in example 6, add instruction writes to the future file before the floating point instruction i.e. is terminated out-of-order [col. 13, under example 6 lines 1-5]); and

d) updating a state of a system processing the instruction to reflect that the instruction has been terminated (results are updated in the future file indicating the instruction has terminated [col. 13, para. 6, lines 5-9]).

10. In regard to claim 2:

11. Smith et al. further disclose that the desirable stage includes an instruction queue (result shift register is an instruction queue, fig. 3b).

12. In regard to claim 3:

13. Smith et al. disclose that the indicating step further includes the step of generating a signal associated with the instruction (functional unit generates a result associated with the instruction [col. 7, para. 4, last 4 lines; fig. 6, result bus]).

14. In regard to claim 4:

15. Smith et al. further disclose the steps of:

a) sending the signal to an early-retirement unit (future file, fig. 6); and

b) the early-retirement unit arranging for the instruction to be terminated (the future file holds the results of the terminating instruction [col. 13, para. 6, lines 5-9]).

16. In regard to claim 5:

17. Smith et al. further disclose that the various processing stages include one or more of the following stages: fetching, issuing, sorting, executing, queuing, and retiring (fig. 1).

18. In regard to claim 6:

19. Smith et al. further disclose that the instruction capable of early retirement (an instruction capable of finishing before an instruction ahead of it i.e. any instruction not at the head of the reorder buffer with valid results [col. 13, example 6, lines 1-8]) includes an identification tag (valid tag in the reorder buffer [fig. 3b] for indicating whether the

instruction has valid results) for identifying whether the instruction is capable of early retirement.

20. In regard to claim 7:

21. Though Smith et al. do not explicitly mention that NO-OP instructions, pre-fetch instructions, branch instructions, nullified instructions, and predicated-false instructions are identified as instructions capable of early retirement, this step is inherent to their processor because **all** instructions are identified as instructions capable of early retirement if their valid tag [fig. 3b] is marked and they are not at the head of the reorder buffer.

22. In regard to claim 8:

23. Smith et al. further disclose that the criteria for early retirement (when an instruction reaches stage 1 of the result shift register [col. 7, para. 4, last 4 lines]) are met when continued processing (writing results of the instruction to correct result register [col. 7, para. 4., last 4 lines]) of the instruction does not change the architectural state (architectural file [col. 13, para. 6, lines 3-5] is not changed as instructions capable of early retirement update the future file [col. 13, para. 6, lines 5-7]) of the system processing the instructions.

24. In regard to claim 9:

25. Smith et al. further disclose that the criteria for early retirement are met (when an instruction reaches stage 1 of the result shift register [col. 7, para. 4, last 4 lines]) when continued processing of the instruction (writing results of the instruction to correct result register [col. 7, para. 4., last 4 lines]) does not change the behavior of the program running the instruction (the results written are of instructions making up the program and hence do not cause the program to behave differently i.e. change its behavior. It should be noted that the applicant has not defined "change of behavior" within the claim itself and hence it is interpreted as to cause the program to behave differently from that which is expected).

26. In regard to claim 19:

27. Smith et al. disclose a system for retiring instructions processed through various processing stages (pipeline stages, fig. 1), comprising:

a) first processing means (pipeline comprising of functional units, fig. 1) for processing an instruction capable of early retirement (pipeline processes instructions capable of retiring out-of-order due to parallel execution of instructions [col. 5, para. 4, lines 1-7]) in functional units with varying execution times [col. 5-6, example 1 indicates varying execution times of the functional units]) until the instruction meets the criteria for early retirement (when an instruction reaches stage 1 of the result shift register [col. 7, para. 4, last 4 lines]);

b) indicating means for indicating that the instruction has met the early-retirement criteria (functional unit result is placed in the correct result register [col. 7, para. 4, last 4 lines]);

c) second processing means for processing the instruction to a desirable stage (result shift register, [col. 7, para. 4]) at which, based on the indication the instruction has met the early-retirement criteria (result is placed in the correct result register, [col. 7, para. 4, last 4 lines]), the instruction is terminated out of order of a program running the instruction (in example 6, add instruction writes to the future file before the floating point instruction i.e. is terminated out-of-order [col. 13, under example 6 lines 1-5]); and

d) updating means (future file, fig. 6) for updating a state of a system processing the instruction to reflect that the instruction has been terminated (results are updated in the future file indicating the instruction has terminated [col. 13, para. 6, lines 5-9]).

28. In regard to claim 20:

29. Smith et al. further disclose that the desirable stage includes an instruction queue (result shift register is an instruction queue, fig. 3b).

Claim Rejections - 35 USC § 103

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

31. Claims **10-18** are rejected under 35 U.S.C. 103(a) for the same reasons as claims 1-9 above as being unpatentable over Smith et al. ("Implementing Precise Interrupts In Pipelined Processors," IEEE Trans. On Comp., Vol. 37, No. 5, May 1988, pp. 562-573) in view of Tannenbaum ("Structured Computer Organization," Prentice-Hall, 1984, pp. 10-12).

32. Smith et al. teaches the claimed elements of 10-18 as detailed in the rejection of claims 1-9 above.

33. Smith et al. differs from the applicant's invention in that it does not teach that instructions on a computer-readable medium embodying instructions that cause a computer to perform the limitations of claims 10-18 of the applicant's invention.

34. However Tannenbaum teaches that any instruction executed by hardware can also be simulated in software (pg 11, para. 4, lines 1-2). He also teaches that hardware

is generally immutable (first para. after sec. 1.4 header) while software allows for more rapid change (pg. 11, para. 4, lines 2-4).

35. One of ordinary skill in the art at the time of the invention would have been motivated to convert the Smith et al. reference to software i.e. instructions on a machine readable medium because Tannebaum teaches that hardware is generally immutable (first para. after sec. 1.4 header) while software allows for more rapid change (pg. 11, para. 4, lines 2-4). Therefore, to allow for ease of correction of mistakes, and/or an ease of addition of new functionality, one of ordinary skill would be motivated to implement the teachings of Smith et al. and Tanenbaum as instructions recorded on a machine readable medium.

36. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the Smith et al. processor by converting it to instructions on a machine-readable medium.

Conclusion

37. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty, which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made.

The applicant or patent owner must also show how the amendments avoid such references or objections. See 37 CFR § 1.111.

a. Aho et al. ("Compilers Principles, Techniques, and Tools, " Addison-Wesley, pp. 530-531) describe dead-code optimization in compilers. It teaches that instructions that are dead, i.e. never subsequently used, can be safely removed.

b. Ronen (US005701442) teaches that NOP instructions have no architectural effect on the processor (col. 4 lines 66-67 col. 5, lines 1-2).

c. Thakkar et al. ("The Internet Streaming SIMD extensions", Intel Technology Journal, Q2, 1999) teaches that prefetch instructions don't update architectural state (pg. 3, col. 2, lines 1-2)

38. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amol V. Gole whose telephone number is 703-305-8888. The examiner can normally be reached on 9:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

RICHARD L. ELLIS
PRIMARY EXAMINER

AVG